IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-7 (Canceled)

Claim 8. (New) A semiconductor memory comprising:

a plurality of memory cells each having a transistor having a source terminal and a drain terminal and a ferroelectric capacitor having a first terminal connected to said source terminal and a second terminal connected to said drain terminal,

wherein said plurality of memory cells are arranged to constitute a cell array.

Claim 9. (New) A memory device according to claim 8, comprising:

wherein a dummy cell in a dummy cell block corresponding to a memory cell block having a transistor, and a ferroelectric or paraelectric capacitor connected between a source and drain terminals of said transistor, said dummy cell block constituted by connecting a plurality of dummy cells in series and connecting at least one first select transistor and at least one second select transistor connected in series to one terminal of said series connected portion, the other terminal of said first select transistor connected to a first bit line, and the other terminal of said second select transistor connected to a second bit line.